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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/657,304	09/08/2003	Kiran K. Gullapalli	SC12003TS	9732

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EXAMINER	
LEVIN, NAUM B	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 05/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/657,304	GULLAPALLI ET AL.	
	Examiner	Art Unit	
	Naum B. Levin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/8/03,2/10/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1-23 are rejected under 35 U.S.C. 102(b) as being unpatentable by Lee (US Patent 6,154,716).

2. As to claims 1, 7, 11 and 22 Lee discloses:

(1) A method of making an integrated circuit, comprising:

defining a model of a circuit for use on the integrated circuit (col.4, ll.33-51);

generating circuit equations of the model (col.3, ll.1-14; col.4, ll.51-55);

determining a steady state response of the model to large signal (noise) excitations (col.2, ll.40-67; col.3, ll.1-14; col.3, ll.34-49);

linearizing about the steady state response to obtain a first order transfer function (col.8, ll.34-43; col.8, ll.65-67; col.9, ll.1-67; col.10, ll.1-14);

determining a first order response of the model (col.5, ll.6-21; col.6, ll.28-59; col.10, ll.15-41);

determining a second order response of the model using the first order transfer function (Discrete Fourier Transform (DFT) by the application of any algorithm such as a

Fast Fourier Transform (FFT) as shown in Fig. 3/inverse as shown in Fig.6) and the first order response (col.5, ll.21-54; col.6, ll.59-60; col.10, ll.41-45);

determining a third order response of the model using the first order transfer function and the second order response (col.5, ll.47-54; col.6, ll.59-67; col.7, ll.1-6; col.10, ll.45-53);

analyzing results of the third order response to determine if the circuit is ready to be manufactured (col.5, ll.55-58; col.7, ll.24-43); and

manufacturing the integrated circuit (col.1, ll.10-20);

(7), (22) A method/computer-readable medium having stored instructions for analyzing a circuit, comprising (col.4, ll.16-31):

generating circuit equations of a model of the circuit (col.3, ll.1-14; col.4, ll.51-55);

deriving a first order transfer function (Discrete Fourier Transform (DFT) by the application of any algorithm such as a Fast Fourier Transform (FFT) as shown in Fig. 3/inverse as shown in Fig.6) of the model (col.5, ll.21-54; col.6, ll.59-60; col.10, ll.41-45);

determining a first order response of the model using the first order transfer function (col.5, ll.6-21; col.6, ll.28-59; col.10, ll.15-41); and

determining a second order response of the model using the first order transfer function and the first order response (col.5, ll.21-54; col.6, ll.59-60; col.10, ll.41-45);

(11) A method of estimating a first solution of a circuit based on first predetermined inputs to the circuit, comprising:

determining a system of equations representing a general solution of the circuit (col.3, ll.1-14; col.4, ll.51-55);

determining a second solution of the circuit based on the general solution at second predetermined inputs (col.8, ll.34-43; col.8, ll.65-67; col.9, ll.1-67; col.10, ll.1-14);

determining a first order transfer function of the general solution at the second predetermined inputs (col.5, ll.21-54; col.6, ll.59-60; col.10, ll.41-45);

solving for a first order estimate of the first solution using the first order transfer function at the second predetermined inputs and the second solution (col.5, ll.21-58; col.6, ll.59-60; col.7, ll.24-43; col.10, ll.41-45); and

solving for a second order estimate of the first solution using the first order transfer function at the second predetermined inputs and the first order estimate (col.5, ll.47-58; col.6, ll.59-67; col.7, ll.1-6; col.7, ll.24-43; col.10, ll.45-53).

3. As to claims 2-6, 8-10, 12-21 and 23 Lee recites:

(2) The method of claim 1, wherein the circuit is an analog circuit (col.1, ll.10-20);

(3), (14) The method, wherein the circuit equations are formulated in the time domain (col.5, ll.6-21);

(4), (15) The method, wherein the circuit equations are formulated in the frequency domain (col.5, ll.21-46);

(5), (16) The method, wherein the circuit equations are formulated as being time-invariant (col.5, ll.47-54);

(6) The method of claim 1, further comprising modifying the circuit design after the step of analyzing and before the step of manufacturing (col.7, ll.24-43);

(8), (23) The method/program, further comprising determining a third order response of the model using the first order transfer function and the second order response (col.5, ll.47-54; col.6, ll.59-67; col.7, ll.1-6; col.10, ll.45-53);

(9) The method of claim 8, further determining a steady state response to large signal excitations of the model, and wherein the step of determining a first order response further comprises using the steady state response (col.2, ll.40-67; col.3, ll.1-14; col.3, ll.34-49);

(10), (17) Using the method to identify shortcomings of the circuit, then modifying the circuit to overcome the shortcomings and manufacturing the circuit as modified (col.5, ll.55-58; col.7, ll.24-43);

(12), (20) The method, further comprising solving for a third order estimate of the first solution using the first order transfer function at the second predetermined inputs and the second order estimate (col.5, ll.47-58; col.6, ll.59-67; col.7, ll.1-6; col.7, ll.24-43; col.10, ll.45-53);

(13), (18) The method, wherein the first solution comprises voltages at nodes within the circuit (col.1, ll.38-54; col.1, ll.64-67; col.2, ll.1-7);

(19), (21) The method, wherein the equations are Kirchoffs laws, and wherein the step of solving for the second order estimate comprises solving a first mathematical formula comprising the first order estimate and a first mathematical expression using the first order transfer function at the second predetermined inputs multiplied by the difference between the first order estimate and the second order estimate (col.1, ll.38-54; col.4, ll.49-67; col.5, ll.1-5).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B. Levin whose telephone number is 571-272-1898. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Naum Levin

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AU-2825